

10/727474

LSI LOGIC

FAX COVER SHEET

LSI LOGIC CORPORATION
Office of General Counsel
1621 Barber Lane
M/S D-106
Milpitas, CA 95035
Fax: (408) 433-7460

RECEIVED
CENTRAL FAX CENTER

NOV 03 2005**Certificate****NOV 08 2005****of Correction**

Date: November 3, 2005
To **Name:** USPTO – MS: Certificate of Correction
Fax: 571-273-8300
Phone: 703-305-8283

From: **Name:** Manu Kashyap, Intellectual Property Paralegal
Corporate Legal Dept.
Telephone: (408) 433-7475
Fax: (408) 433-7460
Re: 6,954,082

Number of Pages Including this Page 4

This facsimile transmission is intended for the addressee indicated above. It may contain information that is privileged, confidential or otherwise protected from disclosure. Any review, dissemination or use of this transmission or its contents by persons other than the addressee is strictly prohibited. If you have received this transmission in error, please notify us immediately by telephone, and mail the original to us at the above address.

MESSAGE:

Docket Number: 03-1681
Box: Certificate of Correction

Please notify us immediately if any pages are not received.

NOV 14 2005

NOV 03 2005

PTO/SB/21 (09-04)

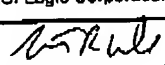
Approved for use through 07/31/2008, OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

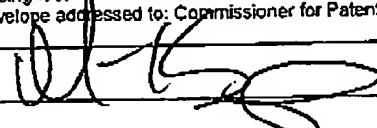
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	6,954,082 B2
	Filing Date	October 11, 2005
	First Named Inventor	Carlo Grilletto
	Art Unit	2829
	Examiner Name	Nguyen, Tu
	Attorney Docket Number	03-1681
Total Number of Pages in This Submission		3

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): Certificate of Correction
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	LSI Logic Corporation		
Signature			
Printed name	Timothy Croll		
Date	November 3, 2005	Reg. No.	36,771

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:	
Signature	
Typed or printed name	Manu Kashyap
Date	November 3, 2005

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NOV 1 2005

PTO/SB/44 (04-05)

Approved for use through 04/30/2007. OMB 0651-0033

U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1PATENT NO. : 6,954,082 B2

APPLICATION NO.: 10/727,474

ISSUE DATE : October 11, 2005

INVENTOR(S) : Carlo Grilletto

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page at column 12, please delete "Grillettc" and replace with - Grilletto -

On the cover page at column 75, please delete "Grillettc" and replace with - Grilletto -

MAILING ADDRESS OF SENDER (Please do not use customer number below):

LSI Logic Corporation
1621 Barber Lane, MS: D-106
Milpitas, CA 95035 U.S.A.

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Should be "Grilletto"



US006954082B2

(12) **United States Patent**
Grilletto

(10) Patent No.: **US 6,954,082 B2**
(45) Date of Patent: **Oct. 11, 2005**

Should Be
"Grilletto"

(54) **METHOD AND APPARATUS FOR TESTING OF INTEGRATED CIRCUIT PACKAGE**

(75) Inventor: Carlo Grilletto, San Carlos, CA (US)

(73) Assignee: LSI Logic Corporation, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/727,474

(22) Filed: Dec. 4, 2003

(65) Prior Publication Data

US 2005/0122127 A1 Jun. 9, 2005

(51) Int. Cl. G01R 31/26

(52) U.S. Cl. 324/765

(58) Field of Search 324/760, 754, 324/755, 757, 765, 158.1, 761, 763

(56) References Cited

U.S. PATENT DOCUMENTS

5,742,168 A 4/1998 Kiyokawa et al. 324/754

6,287,878 B1 9/2001 Maeng et al. 433/15
6,597,189 B1 7/2003 Grilletto
6,750,646 B1 6/2004 Voss et al. 324/158.1

OTHER PUBLICATIONS

IPC-9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," IPC—Association Connecting Electronics Industries, cover page.

* cited by examiner

Primary Examiner—Vinh Nguyen

Assistant Examiner—Tung X. Nguyen

(74) Attorney, Agent, or Firm—L. Jon Lindsay

(57) ABSTRACT

A method and apparatus for testing an integrated circuit (IC) package includes a printed circuit board (PCB) on which is mounted the IC package and which is removably connected (preferably perpendicular) to a motherboard. The IC package, the PCB and the motherboard are subjected to thermal, humidity and/or electrical test conditions.

20 Claims, 4 Drawing Sheets

